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Correctness of Binary Counter Circuits

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Summary. This article introduces the verification of the correctness for the operations and the specification of the 3-bit counter. Both cases: without reset input and with reset input are considered. The proof was proposed by Y. Nakamura in [1].

MML Identifier: `GATE_2`.

The paper [1] provides the terminology and notation for this paper.

In this paper a, b, c, d denote sets.

Next we state four propositions:

(1) Let s_0, s_1, s_2, s_3, s_4, s_5, s_6, s_7, n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7, q_1, q_2, q_3, n_8, n_9, n_{10} be sets such that NE s_0 iff NE AND3(NOT1 q_3, NOT1 q_2, NOT1 q_1) and NE s_1 iff NE AND3(NOT1 q_3, NOT1 q_2, q_1) and NE s_2 iff NE AND3(NOT1 q_3, q_2, NOT1 q_1) and NE s_3 iff NE AND3(NOT1 q_3, q_2, q_1) and NE s_4 iff NE AND3(q_3, NOT1 q_2, NOT1 q_1) and NE s_5 iff NE AND3(q_3, NOT1 q_2, q_1) and NE s_6 iff NE AND3(q_3, q_2, NOT1 q_1) and NE s_7 iff NE AND3(q_3, q_2, q_1) and NE n_0 iff NE AND3(NOT1 n_{10}, NOT1 n_9, NOT1 n_8) and NE n_1 iff NE AND3(NOT1 n_{10}, NOT1 n_9, n_8) and NE n_2 iff NE AND3(NOT1 n_{10}, n_9, NOT1 n_8) and NE n_3 iff NE AND3(NOT1 n_{10}, n_9, n_8) and NE n_4 iff NE AND3(n_{10}, NOT1 n_9, NOT1 n_8) and NE n_5 iff NE AND3(n_{10}, NOT1 n_9, n_8) and NE n_6 iff NE AND3(n_{10}, n_9, NOT1 n_8) and NE n_7 iff NE AND3(n_{10}, n_9, n_8) and NE n_8 iff NE NOT1 q_1 and NE n_9 iff NE XOR2(q_1, q_2) and NE n_{10} iff NE OR2(AND2(q_3, NOT1 q_1), AND2(q_1, XOR2(q_2, q_3))). Then

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(i) NE n_1 iff NE s_0,
(ii) NE n_2 iff NE s_1,
(iii) NE n_3 iff NE s_2,
(iv) NE n_4 iff NE s_3,
(v) NE n_5 iff NE s_4,
(vi) NE n_6 iff NE s_5,
(vii) NE n_7 iff NE s_6, and
(viii) NE n_0 iff NE s_7.

(2) NE $\mathrm{AND3}(\mathrm{AND2}(a,d),\mathrm{AND2}(b,d),\mathrm{AND2}(c,d))$ iff NE $\mathrm{AND2}(\mathrm{AND3}(a,b,c),d)$.

(3)(i) Not NE $\mathrm{AND2}(a,b)$ iff NE $\mathrm{OR2}(\mathrm{NOT1}\,a,\mathrm{NOT1}\,b)$,
(ii) NE $\mathrm{OR2}(a,b)$ and NE $\mathrm{OR2}(c,b)$ iff NE $\mathrm{OR2}(\mathrm{AND2}(a,c),b)$,
(iii) NE $\mathrm{OR2}(a,b)$ and NE $\mathrm{OR2}(c,b)$ and NE $\mathrm{OR2}(d,b)$ iff NE $\mathrm{OR2}(\mathrm{AND3}(a,c,d),b)$, and
(iv) if NE $\mathrm{OR2}(a,b)$ and NE a iff NE c, then NE $\mathrm{OR2}(c,b)$.

(4) Let s_0, s_1, s_2, s_3, s_4, s_5, s_6, s_7, n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7, q_1, q_2, q_3, n_8, n_9, n_{10}, R be sets such that NE s_0 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,q_3,\mathrm{NOT1}\,q_2,\mathrm{NOT1}\,q_1)$ and NE s_1 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,q_3,\mathrm{NOT1}\,q_2,q_1)$ and NE s_2 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,q_3,q_2,\mathrm{NOT1}\,q_1)$ and NE s_3 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,q_3,q_2,q_1)$ and NE s_4 iff NE $\mathrm{AND3}(q_3,\mathrm{NOT1}\,q_2,\mathrm{NOT1}\,q_1)$ and NE s_5 iff NE $\mathrm{AND3}(q_3,\mathrm{NOT1}\,q_2,q_1)$ and NE s_6 iff NE $\mathrm{AND3}(q_3,q_2,\mathrm{NOT1}\,q_1)$ and NE s_7 iff NE $\mathrm{AND3}(q_3,q_2,q_1)$ and NE n_0 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,n_{10},\mathrm{NOT1}\,n_9,\mathrm{NOT1}\,n_8)$ and NE n_1 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,n_{10},\mathrm{NOT1}\,n_9,n_8)$ and NE n_2 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,n_{10},n_9,\mathrm{NOT1}\,n_8)$ and NE n_3 iff NE $\mathrm{AND3}(\mathrm{NOT1}\,n_{10},n_9,n_8)$ and NE n_4 iff NE $\mathrm{AND3}(n_{10},\mathrm{NOT1}\,n_9,\mathrm{NOT1}\,n_8)$ and NE n_5 iff NE $\mathrm{AND3}(n_{10},\mathrm{NOT1}\,n_9,n_8)$ and NE n_6 iff NE $\mathrm{AND3}(n_{10},n_9,\mathrm{NOT1}\,n_8)$ and NE n_7 iff NE $\mathrm{AND3}(n_{10},n_9,n_8)$ and NE n_8 iff NE $\mathrm{AND2}(\mathrm{NOT1}\,q_1,R)$ and NE n_9 iff NE $\mathrm{AND2}(\mathrm{XOR2}(q_1,q_2),R)$ and NE n_{10} iff NE $\mathrm{AND2}(\mathrm{OR2}(\mathrm{AND2}(q_3,\mathrm{NOT1}\,q_1),\mathrm{AND2}(q_1,\mathrm{XOR2}(q_2,q_3))),R)$. Then

(i) NE n_1 iff NE $\mathrm{AND2}(s_0,R)$,
(ii) NE n_2 iff NE $\mathrm{AND2}(s_1,R)$,
(iii) NE n_3 iff NE $\mathrm{AND2}(s_2,R)$,
(iv) NE n_4 iff NE $\mathrm{AND2}(s_3,R)$,
(v) NE n_5 iff NE $\mathrm{AND2}(s_4,R)$,
(vi) NE n_6 iff NE $\mathrm{AND2}(s_5,R)$,
(vii) NE n_7 iff NE $\mathrm{AND2}(s_6,R)$, and
(viii) NE n_0 iff NE $\mathrm{OR2}(s_7,\mathrm{NOT1}\,R)$.

References

[1] Yatsuka Nakamura. Logic gates and logical equivalence of adders. *Formalized Mathematics*, 8(**1**):35–45, 1999.

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